

Intel Next Generation Multi-core Platforms

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Agenda

- **Multi-core Project Update**
- **Multi-core Benefit Review**
- **Intel Next Generation Micro-architecture**
- **Intel Enabling and Manufacturing**
- **Summary**

Intel PLATFORM....and Multi-core

Platform Strategies: Across All Segments & Driven by User Needs



DIGITAL HOME



DIGITAL ENTERPRISE



MOBILITY



DIGITAL HEALTH



CHANNEL

Battery Life/Power

Connectivity

Security

.....

Compute Capability

Manageability

Form Factor

Intel Multi-core: Platform element delivering tremendous growth in **Compute Capability**

- Building upon success of HT Technology
- Better **Multitasking Responsiveness**
- Improved **Multi-threading performance**

The Move to Intel Multi-core

Platform

2005

2006

2007+

Itanium® processor	Itanium® 2 Processor	Montecito	Montvale	Tukwila Poulson Dimona
MP Server	64-bit Intel® Xeon™ processor MP	PaxvilleMP	Tulsa	Whitefield
DP Server / WS	64-bit Intel® Xeon™ Processor w/ 2MB cache	PaxvilleDP Dempsey Sossaman	Woodcrest	
Desktop Client	Pentium® 4 processor	Pentium® Processor Extreme Edition Pentium® D Processor	Presler Conroe	
		Pentium® 4 processor	Cedar Mill	
Mobile Client	Pentium® M processor		Yonah Merom	
			Yonah	

today



All products and dates are preliminary and subject to change without notice.

Refer to 'fact sheet' for specific product timings

Single core

Multi-core
(≥2 cores)

Multi-core
(≥4cores)

Multi-core Everywhere: > 15 Projects

	2005	2006**	2007**
Desktop Performance*	Shipping	>70%	>90%
Mobile Performance*	Shipping	>70%	>90%
Server	Shipping	>85%	~100%



Desktop Client



Mobile client



Server & Workstation

* Mobile & Desktop Pentium

** Data is projected run rate exiting the year. Source: Intel

**Aligned with Strong Platforms
Broadly Delivering Benefits of Parallelism**

Greater Performance &

Lower Energy Consumption



Multi-tasking Responsiveness



Greater App Performance



Higher Compute Density

Smaller DT Platforms



Mobility: On the go



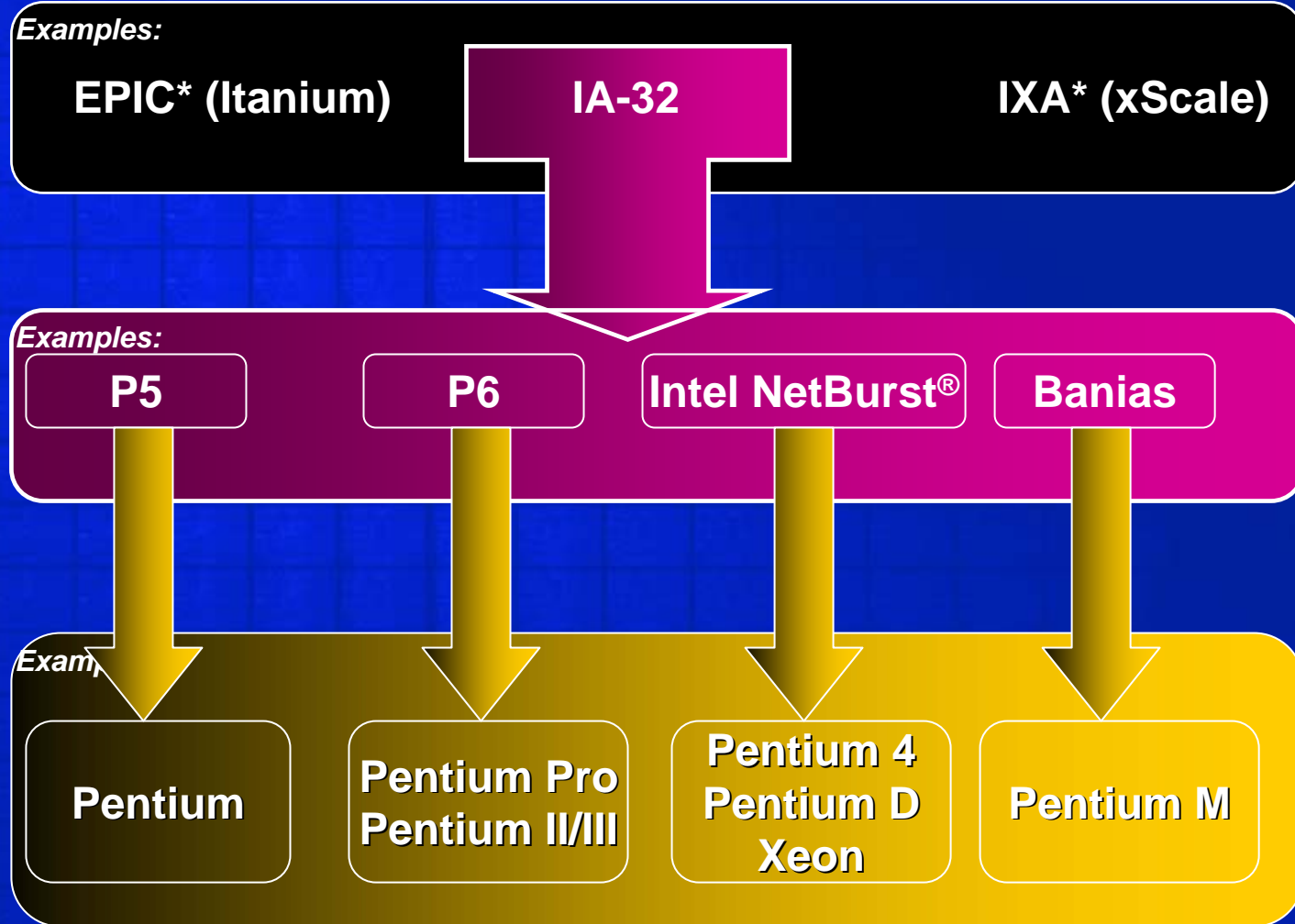
..... Greater Power Efficiency

Micro-architecture History

Architecture:
Instruction set definition
and compatibility

**Micro-
Architecture:**
Hardware implementation
maintaining instruction
set compatibility with
high-level architecture

Processors:
Productized
implementation of
micro-architecture



Intel's Next Generation Micro-Architecture

Architecture:

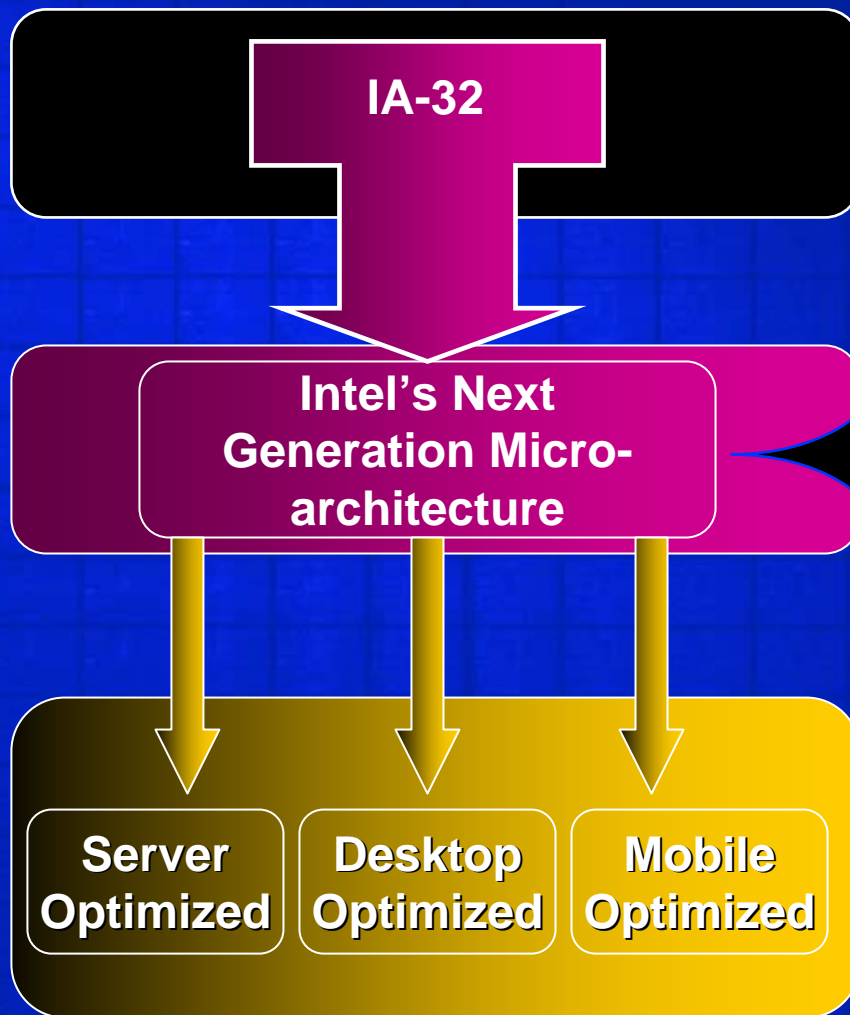
Instruction set definition and compatibility

Micro-Architecture:

Hardware implementation maintaining instruction set compatibility with high-level architecture

Processors:

Productized implementation of micro-architecture



Low Power

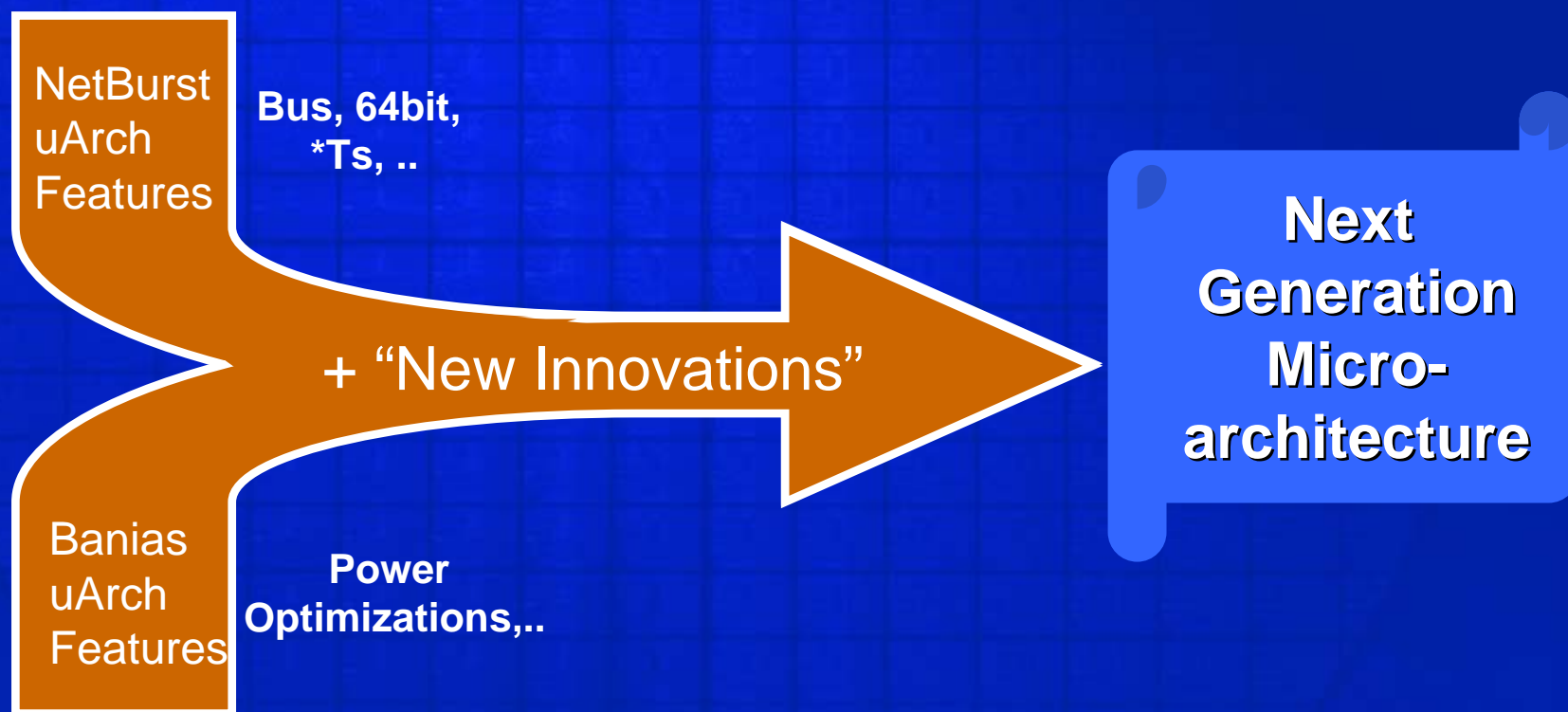
High Performance

Scalable

Foundation for Innovation

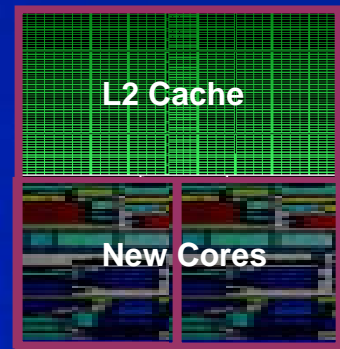
Intel's Next Generation Micro-architecture**

- Combining targeted features of existing micro-architectures
- Adding new, user valued, innovations



Intel's Next Generation Micro-architecture**

- **Higher Performance OOO** (out of order) **Engine****
 - Wider (4 issue); Deeper Buffers; 14 Stage Efficient Pipeline
- **Advanced Power Capability****
 - Architected for Power Efficiency
- **Multi-core Enhanced Cache System****
 - Shared & scalable L2 Cache
 - Direct L1 to L1 cache transfer; Higher relative L2-core BW;
- **Improved Memory Access****
 - Improved Pre-fetch, Memory Disambiguation



*Not representative of actual die photo or relative size

New and Innovative Features

Delivering Awesome Performance & Power Efficiency

Example: Server

64-bit Intel® Xeon™ Processor Roadmap

Single Core

1H'06

2H'06

Performance /
Watt

Up to 3.5X
PERFORMANCE/
WATT**

Performance

Over 2X
PERFORMANCE**

Intel Next Generation
Micro-architecture
based platform

*Graphics not representative of actual die photo or relative size

With Intel Next Generation Micro-architecture



Platform Scalable Micro-Architecture

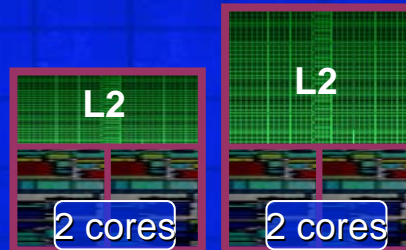
Mobile Platform

Merom Family



Desktop Platform

Conroe Family

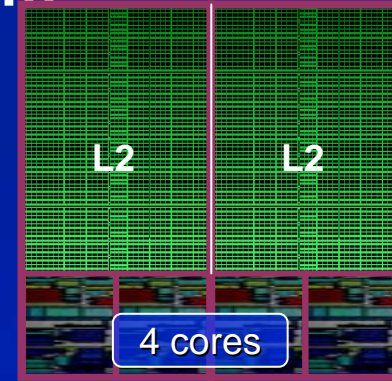


Server Platform

Woodcrest



Whitefield



Mobile Optimized

- Mobility TDP Envelope
- Mobile Platform FFs
- 2 Execution Cores – 65nm
- Mobile Power Optimizations
- Mobile Client *Ts

Desktop Optimized

- 65W Target TDP
- Smaller Desktop Platform FFs
- 2 Execution Cores – 65nm
- Multiple L2 Cache Sizes
- Desktop Client *Ts

Server Optimized

- ~40% reduction in TDP
- Smaller Server Platform FFs
- 2 to 4 Execution Cores – 65nm
- Wide Range of L2 Cache Sizes
- Server *Ts
- DP/MP support

Next Generation Micro-architecture**

Single Micro-architecture – Feature Optimized Per Product

**Micro-Architecture Name TBD

*Graphics not representative of actual die photo or relative size

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The IA Multi-core Platforms

Platform

2006

2007

MP Servers

Montecito / Montvale
Intel® E8870 Chipset / Enabled

Richford / Future Platform
Tukwila(07) / Poulson
Future Chipset

Millington / DP Montvale
Intel® E8870 Chipset / Enabled

Truland Platform
Paxville
Intel® E8500 Chipset

Reidland Platform (2007)
Whitefield (2-4core) (2007)

DP Servers

Bensley Platform (Q1'06)
Woodcrest (2H'06)

DP Workstation

Glidewell Platform (Q1'06)
Woodcrest (2H'06)

UP Server

Desktop -Home

Bridge Creek Platform (Mid'06)
Conroe (2H'06)

Desktop -Office

Averill Platform (mid'06)
Conroe (2H'06)

Mobile Client

Napa Platform (Q1'06)
Merom (2H'06)



All products and dates are preliminary and subject to change without notice.

Note: only multi-core processors listed 14

Intel's Software Advantage

6 divisions • 24 major sites • 3,000+ employees

Accelerate Industry
Knowledge & Experience



Software Vendor
Alliances

Easy Access To
Advanced Technology



Intel® Early
Access Program

Boost SW Performance
– on Any Platform



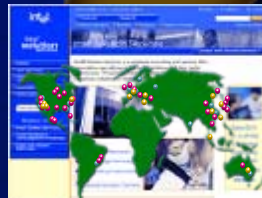
Intel® Software Tools

'One-Stop Shop'
For Developers

Intel® software network

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Network
www.intel.com/software

Business &
Technology Services



Intel® Solutions
Services

Advanced
Technical Training

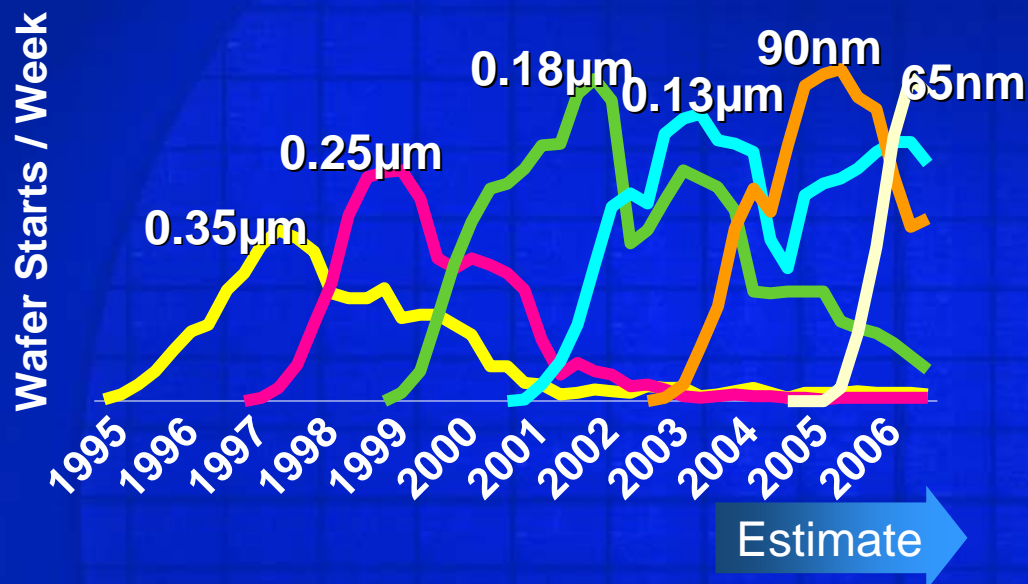


Intel® Software
College

Cultivating the Path to Parallelism

- **Tools:** Development of Suite of Threading Tools
 - Thread Checker & Thread Profiler
 - All Intel tools tuned for threading (Vtune™, Compilers, IPP, etc)
 - Software Development platforms
- **Education:** Development of Threading Curriculum
 - Used within Intel Software College and with Universities
 - 150 Certified Expert Instructors World Wide
 - On-line and Instructor Led Courses
- **Threading Community:** Intel Software Network
 - Threading Knowledge Base
 - Community Forum: Threading on Parallel Architectures
 - Case Studies, White Papers, Code Samples
 - www.intel.com/software

Intel's Technology & Manufacturing Pipeline

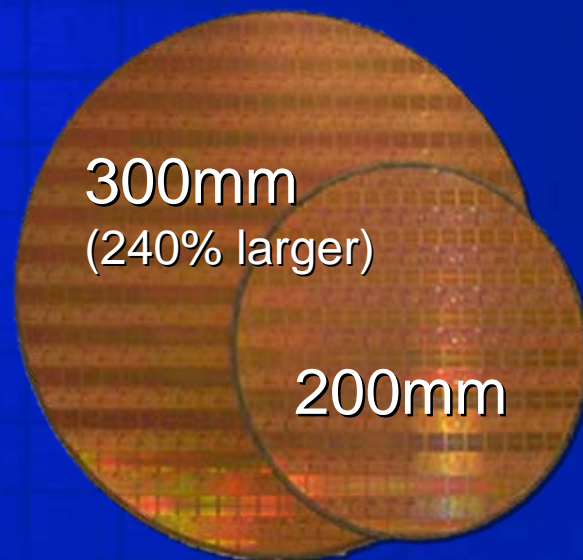


Process Technology in 2005

- 90nm conversion completed
- 65nm ramp starts/ Faster ramp than 90nm

300mm Factories

- 4 300mm factories online today
- Fab 12 (Arizona) online in 2H 2005
- Fab 24 (Ireland) expansion in early 2006
- Fab 32 (Arizona) in 2007



Delivering the Benefits of Multi-core in Volume

Summary

- **New consumer and IT-focused benefits, inside Intel platforms, advancing the computing experience**
- **Intel Multi-core roadmap remains on track**
 - Paxville MP and DP accelerated
- **Next generation micro-architecture optimized for power efficiency**
 - Higher performance, low power and scalability
- **Multi-core software enabling program accelerating ‘time-to-value’ for end user and ecosystem**
- **Capacity to broadly deliver benefits of parallelism**

Backup

- **For more information, please contact**
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